RN0238

Release Notes

CoreVectorBlox

November 2020

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in November 2020. The following is the list of changes in revision 2.0.

- The version number was updated from v0.9 to v1.0
- *Release History* table was updated

1.2 Revision 1.0

Revision 1.0 was published in June 2020. It is the first publication of this document.

2 About This Release

This document accompanies the production release of CoreVectorBlox v1.0 IP core. It describes its features and enhancements. It also contains the information on system requirements, supported families, implementations, known limitations and workarounds, and resolved issues from the previous version.

2.1 Documentation

For more information about Microsemi Intellectual Property, visit *http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores*.

For updates and additional information about Microsemi software, FPGAs, and hardware, visit *http://www.microsemi.com*.

2.2 Release History

The following table lists the release history of this core.

Table 1 • CoreVectorBlox Release History

Version	Date	Changes
0.9	June 2020	Initial release.
1.0	November 2020	Performance improvements. Added output_valid interrupt signal.

2.3 Features

CoreVectorBlox is a highly configurable core and has the following features:

- Multiple preset configurations to trade-off performance for resource utilization
- Overlay design allows multiple networks to run on the same core, even switch dynamically
- Configurable width (64-bit to 256-bit) AXI4 memory master for data access
- AXI4-Lite slave for control and status
- Memory-based; reads inputs from and writes outputs to memory-mapped master
- Internal vector processor, which can process general neural-network layers
- CNN accelerator for convolutional layers

2.4 Delivery Types

CoreVectorBlox is licensed as encrypted Register Transfer Level (RTL). Encrypted RTL source code is provided for the core.

2.5 Supported Families

This section lists the families supporting CoreVectorBlox v1.0 IP core:

- PolarFire®

2.6 Supported Tool Flows

Libero® System-on-Chip (SoC) v12.3 or later must be used with this CoreVectorBlox release.

2.7 Installation Instructions

Within the Libero SoC software, click Add Core to Vault under the Catalog tab to locate and install a local CPZ file, or use the automatic web update feature in the Libero SoC. Once the CPZ file is installed in Libero SoC, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero SoC project.

See *Libero online help* for further instructions on core instantiation, licensing, and general use.

3 What is New?

3.1 New Features and Devices

This is the initial CoreVectorBlox release.

3.2 Known Issues and Workarounds

There are no known limitations or workarounds in CoreVectorBlox v1.0.

3.3 Discontinued Features and Devices

There are no discontinued features in the v1.0 release.

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